In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

1. (Original) An integrated circuit comprising:

a digital-to-analogue converter (DAC),

a clear code register for storing a digital clear code, and

a control circuit responsive to a clear signal for transferring the clear code from the clear code register to the DAC, so that the DAC outputs an analogue output signal corresponding to the clear code in the clear condition.

2. (Original) An integrated circuit as claimed in claim 1 in which the integrated circuit comprises a plurality of channels, a DAC being provided in each channel.

3. (Original) An integrated circuit as claimed in claim 2 in which the control circuit is responsive to the clear signal for transferring the clear code from the clear code register to at least some of the DACs.

4. (Original) An integrated circuit as claimed in claim 2 in which the control circuit is responsive to the clear signal for transferring the clear code from the clear code register to each of the DACs.

5. (Original) An integrated circuit as claimed in claim 2 in which a plurality of clear code registers are provided for storing clear codes for corresponding ones of at least some of the DACs, the control circuit being responsive to the clear signal for transferring the clear codes from the respective clear code registers to the corresponding DACs.

6. (Original) An integrated circuit as claimed in claim 5 in which the number of DACs is greater than the number of clear code registers, and at least some of the clear code registers store the clear codes for respective pluralities of corresponding DACs.

7. (Original) An integrated circuit as claimed in claim 5 in which a clear code register is provided for each DAC for storing a clear code for the corresponding DAC.

8. (Previously presented) An integrated circuit as claimed in claim 5 in which each clear code register is programmable.

9. (Original) An integrated circuit as claimed in claim 8 in which each clear code register is programmable independently of the other clear code registers.

10. (Previously presented) An integrated circuit as claimed in claim 2 in which a DAC register is provided corresponding to each DAC for sequentially storing digital words to be sequentially converted by the DAC, and the control circuit is responsive to the clear signal for transferring the clear code from the clear code register of the corresponding DAC to the corresponding DAC register.

11. (Original) An integrated circuit as claimed in claim 1 in which an input terminal is provided for receiving the clear signal as an externally generated clear signal.

12. (Previously presented) An integrated circuit as claimed in claim 5 in which the clear code stored in each clear code register is of value for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel to be of a predetermined analogue value.

13. (Previously presented) An integrated circuit as claimed in claim 5 in which the clear code stored in each clear code register is of value for providing the analogue output signal

outputted by the corresponding DAC on an analogue output terminal of the corresponding channel to be of a predetermined analogue voltage value.

14. (Previously presented) An integrated circuit as claimed in claim 5 in which the clear code stored in each clear code register is of value for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel to be of zero volts.

15. (Previously presented) An integrated circuit as claimed in claim 5 in which the clear code stored in each clear code register is of value for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel with correction for voltage offset in the DAC.

16. (Previously presented) An integrated circuit as claimed in claim 5 in which the clear code stored in each clear code register is of value for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel with correction for voltage offset in the channel.

17. (Original) A multi-channel integrated circuit comprising:

a plurality of channels,

a DAC located in each channel,

a plurality of clear code registers for storing digital clear codes for respective ones of at least some of the DACs, and

a control circuit responsive to a clear signal for transferring the clear codes from the clear code registers to the corresponding DACs, so that the corresponding DACs output an analogue output signal corresponding to the clear codes in the clear code condition.

18. (Original) A multi-channel integrated circuit as claimed in claim 17 in which one clear code register is provided for each DAC.

19. (Original) A method for setting a DAC of an integrated circuit to a clear condition in response to a clear signal, the method comprising the steps of:

providing a clear code register in the integrated circuit,

storing a clear code in the clear code register, and

transferring the clear code from the clear code register to the DAC in response to the clear signal so that the DAC outputs an analogue output signal corresponding to the clear code in the clear condition.

20. (Original) A method as claimed in claim 19 in which the clear code is written to the clear code register.

21. (Original) A method as claimed in claim 19 in which the integrated circuit comprises a plurality of channels with one DAC being located in each channel, and the method comprises the step of transferring the clear code from the clear code register in response to the clear signal to at least one of the DACs.

22. (Original) A method as claimed in claim 21 in which the clear code is transferred to each of the DACs in response to the clear signal.

23. (Original) A method as claimed in claim 21 in which a plurality of clear code registers are provided, and clear codes for corresponding ones of at least some of the DACs are stored in the clear code registers.

24. (Original) A method as claimed in claim 23 in which the number of clear code registers is less than the number of DACs, and at least some of the clear code registers store the clear codes for respective corresponding pluralities of the DACs.

25. (Original) A method as claimed in claim 23 in which a clear code register is provided for each DAC.

26. (Original) A method as claimed in claim 23 in which the clear codes are written to the respective clear code registers independently of each other.

27. (Original) A method as claimed in claim 19 in which each clear code register is provided as a programmable register.

28. (Previously presented) A method as claimed in claim 23 in which the clear code for each clear code register is selected for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel to be of a predetermined analogue value.

29. (Previously presented) A method as claimed in claim 23 in which the clear code for each clear code register is selected for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel to be of a predetermined analogue voltage value.

30. (Previously presented) A method as claimed in claim 23 in which the clear code for each clear code register is selected for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel to be of zero volts.

31. (Previously presented) A method as claimed in claim 23 in which the clear code for each clear code register is selected for providing the analogue output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel with correction for voltage offset in the DAC.

32. (Previously presented) A method as claimed in claim 23 in which the clear code for each clear code register is selected for providing the output signal outputted by the corresponding DAC on an analogue output terminal of the corresponding channel with correction for voltage offset in the channel.

33. (Previously presented) A method as claimed in claim 21 in which a DAC register is provided corresponding to each DAC for sequentially storing respective digital words to be sequentially converted by the DAC, and the clear code from the corresponding clear code register is written to the DAC register of the corresponding DAC in response to the clear signal.

34. (Original) A method as claimed in claim 19 in which the clear signal is an externally generated signal and is applied to the integrated circuit.

35. (New) An integrated circuit as claimed in claim 1 in which the clear code register is programmable.

36. (Currently amended) An integrated circuit as claimed in Claim 1 in which the clear code stored in the clear code register is of value for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ to be of a predetermined analogue value.

37. (Currently amended) An integrated circuit as claimed in Claim 1 in which the clear code stored in the clear code register is of value for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ to be of a predetermined analogue voltage value.

38. (Currently amended) An integrated circuit as claimed in Claim 1 in which the clear code stored in the clear code register is of value for providing the analogue output signal outputted by the ~~corresponding~~ DAC ~~on an analogue output terminal of the channel~~ to be of zero volts.

39. (Currently amended) An integrated circuit as claimed in Claim 1 in which the clear code stored in the clear code register is of value for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ with correction for voltage offset in the DAC.

40. (Currently amended) An integrated circuit as claimed in Claim 1 in which the clear code stored in the clear code register is of value for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ with correction for voltage offset in ~~the~~ a channel[[.]] in which the DAC is provided.

41. (Previously presented) An integrated circuit as claimed in claim 1 in which a DAC register is provided for sequentially storing digital words to be sequentially converted by the DAC, and the control circuit is responsive to the clear signal for transferring the clear code from the clear code register to the DAC register.

42. (Currently amended) A method as claimed in Claim 19 in which the clear code for the clear code register is selected for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ to be of a predetermined analogue value.

43. (Currently amended) A method as claimed in Claim 19 in which the clear code for the clear code register is selected for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ to be of zero volts.

44. (Currently amended) A method as claimed in Claim 19 in which the clear code for the clear code register is selected for providing the analogue output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ with correction for voltage offset in the DAC.

45. (Currently amended) A method as claimed in Claim 19 in which the clear code for the clear code register is selected for providing the output signal outputted by the DAC ~~on an analogue output terminal of the channel~~ with correction for voltage offset in ~~the~~ a channel[[.]] in which the DAC is provided.

46. (Previously presented) A method as claimed in claim 19 in which a DAC register is provided for sequentially storing digital words to be sequentially converted by the DAC, and the clear code from the clear code register is written to the DAC register in response to the clear

signal.